PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Koji YAMAGUCHI

Attn: OFFICE OF PUBLICATIONS

Notice of Allowance
Mailed: May 8, 2006

Batch No.: 6391

Application No.: 10/753,357

Group Art Unit: 2822

Filed: January 9, 2004

Examiner: R. POTTER

Docket No.: 118292

For: WIRING SUBSTRATE, SEMICONDUCTOR DEVICE, SEMICONDUCTOR MODULE, ELECTRONIC EQUIPMENT, METHOD FOR DESIGNING WIRING SUBSTRATE, METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE, AND METHOD FOR MANUFACTURING SEMINCONDUCTOR MODULE

REQUEST FOR ACKNOWLEDGMENT OF CONSIDERATION OF DISCLOSED INFORMATION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

An Information Disclosure Statement with Form PTO-1449 was filed in the above-captioned patent application on June 5, 2006. A copy of the stamped postcard receipt is attached. Applicants have not yet received back from the Examiner a copy of the Form PTO-1449 initialed to acknowledge the fact that the Examiner has considered the cited disclosed information.

The Examiner is requested to initial and return to the undersigned a copy of the subject Form PTO-1449. For the convenience of the Examiner, a copy of that form is attached.

Should there be any questions concerning this communication, please telephone the undersigned at the number set forth below.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Gang Luo
Registration No. 50,559

JAO:GXL/sqb
Date: June 12, 2006

OLIFF & BERRIDGE, PLC
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Alexandria, Virginia 22320
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DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
Charge any fee due to our Deposit Account No. 15-0461

Docket Slip ID: P-2675

PTO RECEIPT FOR FILING OF PAPERS

The following papers have been filed:

Information Disclosure Statement, Check no. 180490 ($180); Form PTO-1449 (6 refs., 6 Engl-lang Abstrs., 2 Engl-land Trnsls.)

Name of Applicant:	Koji YAMAGUCHI
Serial No.:	10/753,357
Attorney File No.:	118292
Title:	Wiring Substrate, Semiconductor Device, Semiconductor Module, Electronic Equipment, Method for Designing Wiring Substrate, Method for Manufacturing Semiconductor Device, and Method for Manufacturing Seminconductor Module
Sender's Initials:	JAO:GXL/eks
Assignee:	SEIKO EPSON CORPORATION

72/45

PATENT OFFICE DATE STAMP

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COPY TO BE STAMPED BY PATENT OFFICE AND RETURNED BY MESSENGER

Form PTO-1449 (REV. 1/06) — US Dept. of Commerce, PATENT & TRADEMARK OFFICE

INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

ATTY DOCKET NO.	APPLICATION NO.
118292	10/753,357
APPLICANT(S): Koji YAMAGUCHI	
FILING DATE: January 9, 2004	GROUP: 2822

U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.	Document Number	Date	Name

FOREIGN PATENT DOCUMENTS

Examiner Initials	Cite No.	Document Number	Date	Country	With English Abstract	With English Translation
	1	JP 2002-289645	10/04/2002	JAPAN	X	X
	2	JP 2000-243862	09/08/2000	JAPAN	X	X
	3	JP 08-055875	02/27/1996	JAPAN	X	
	4	JP 09-298254	11/18/1997	JAPAN	X	
	5	JP 10-256428	09/25/1998	JAPAN	X	
	6	JP 2000-133668	05/12/2000	JAPAN	X	

OTHER DOCUMENTS

Examiner Initials	Cite No.	(Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER | DATE CONSIDERED

Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Date: June 5, 2006